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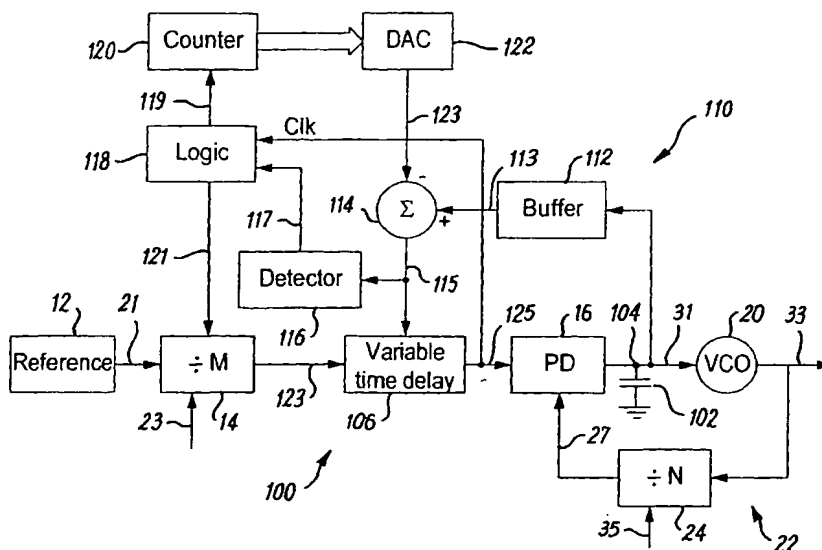
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0230289.1 30 December 2002 (30.12.2002) GB</p> <p>(71) Applicant (for all designated States except US): NOKIA CORPORATION [FI/FI]; Keilalahdentie 4, FIN-02150 Espoo (FI).</p> <p>(72) Inventor; and</p> <p>(75) Inventor/Applicant (for US only): BEESON, Peter [GB/GB]; 16 Haywards Close, Henley-on-Thames, Oxon RG9 1UY (GB).</p> <p>(74) Agent: HIGGIN, Paul; Swindell & Pearson, 48 Friar Gate, Derby DE1 1GY (GB).</p> | <p>(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.</p> <p>(84) Designated States (regional): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published:
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(54) Title: IMPROVED PHASE LOCKED LOOP



(57) **Abstract:** A phase locked loop circuit, for providing an oscillating output signal at an output frequency, comprising: a reference counter; a loop counter; a phase detector having a first input coupled to the reference counter and second input coupled to the loop counter; a voltage controlled oscillator having an input coupled to the output of the phase detector and an output for providing the oscillating output signal; a feedback loop coupling the output of the voltage controlled oscillator to the input of the loop counter; and delay circuitry, including a feedback loop, arranged to introduce a discrete delay into the output of the loop counter and/or the reference counter.

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